UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,402	01/11/2002	Olivier Menut	00-GR1-239	8917

23334 7590 07/30/2004

FLEIT, KAIN, GIBBONS, GUTMAN, BONGINI
& BIANCO P.L.
ONE BOCA COMMERCE CENTER
551 NORTHWEST 77TH STREET, SUITE 111
BOCA RATON, FL 33487

EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,402	MENUT ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,15 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher et al. (USPAT 4942554, Kircher) in view of Jang et al. (USPAT 5637529, Jang).

With regard to claim 1, Kircher discloses a process for fabricating a semiconductor substrate with a single crystal lattice. Kircher discloses in figures 1 – 5 forming a substrate (1) with a single crystal lattice, the substrate having a top surface with at least one discontinuity in the single crystal lattice therein, whereby the top surface of the substrate has a recess (2) at the discontinuity on the top surface. Kircher does not teach amorphizing the single crystal lattice around a periphery of the recess. Jang teaches in figure 1b amorphizing a single crystal lattice (31) around a periphery of a recess (39). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the amorphizing of Jang in the method of Kircher in order to remove lattice defects, thereby improving yield and productivity of the semiconductor device as stated by Jang in column 1, lines 45 – 50. Kircher discloses in figures 1 – 5 depositing a layer of amorphous material (8) having the same chemical composition as that of the substrate. It would have been further obvious in the method of Kircher and Jang that the

depositing the layer of amorphous material would be performed on the structure obtained after amorphizing in order to take advantage of the amorphization of Jang and the amorphous layer of Kircher before any annealing step is performed (see Kircher column 4, lines 13 – 20 and Jang column 2, lines 49 – 60). Kircher discloses in figures 1 – 5 and column 4, lines 13 – 20 thermally annealing the amorphous material so as to be continuous with the single crystal lattice of the substrate.

With regard to claim 2, Kircher discloses in column 4, lines 6 and 7 planarizing the top surface of the substrate.

With regard to claim 4, Kircher discloses in column 3, line 44 wherein the step of forming the substrate includes forming the substrate with at least part of the material of silicon.

With regard to claim 17, Kircher and Jang disclose an integrated circuit comprising a silicon substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface and whereby the surface is treated in accordance with the process of claim 1.

3. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher and Jang as applied to claims 1 and 2 above, and further in view of Tan et al. (USPAT 6001706, Tan).

With regard to 3, Kircher teaches a step of planarizing in column 4, lines 6 and 7. Kircher does not teach how the planarization is accomplished. Tan teaches in figure 10a and column 5, lines 53 – 58 wherein a step of planarizing a top surface includes planarizing the top

surface by a chemical mechanical polishing. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the chemical mechanical polishing of Tan in the method of Kircher and Jang in order to reliably produce a planar substrate thus improving device yields and device performance.

With regard to claim 5, Jang teaches in column 2, lines 50 – 60 wherein the step of amorphizing includes amorphizing with a localized ion implantation around the recess by a masking operation.

4. Claims 6 – 10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kircher and Jang as applied to claims 1 and 2 above, and further in view of Lill et al. (USPAT 6074954, Lill) and Numazawa et al. (USPAT 6168996, Numazawa).

With regard to claim 6, Kircher discloses in figures 1 – 5 wherein the step of forming a substrate include the sub-steps of etching a trench, and filling trench with a fill material so as to form the single-crystal lattice discontinuity. Kircher does not teach depositing first and second layers. Lill teaches in figures 3 – 13b depositing a first layer (6) of a first material and a second layer (8) of a second material in succession on a substrate (2), etching the first layer and an upper portion of a trench fill material (16) so as to form lateral cavities (22) in the second layer in communication with a trench (16) and so as to form the recess at a discontinuity (12). It would have been obvious to one of ordinary skill in the art to use the first and second layers of Lill in the method of Kircher and Jang in order to provide a mask for the etching of the trench as taught by Lill in column 10, line 56 – column 11, line 37. Kircher, Jang and Lill are silent to removing the second layer. Numazawa teaches in figures 21 and 22 removing a second layer (2b) it would

have been obvious to one of ordinary skill in the art at the time of the present invention to use the removing of Numazawa in the method of Kircher, Jang and Lill in order to expose underlying layers for the production of devices that will communicate with the trench.

With regard to claim 7, Kircher discloses in figure 2 wherein the sub-step of filling of the trench with fill material includes filling the trench with at least part of the fill material of a silicon oxide (4).

With regard to claim 8, Kircher discloses in figure 2 wherein the sub-step of filling of the trench with fill material includes filling at least part of the trench with an insulating fill material.

With regard to claim 9, Lill teaches in figure 4, and column 11, liens 51 – 62 wherein a sub-step of filling the trench is carried out by depositing silicon oxide (10) as a conformal coating. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conformal coating of Lill in order to form a dielectric layer with a defect density low enough for improved performance of DRAM devices.

With regard to claim 10, Numazawa teaches in figure 19 wherein the sub-step of filling of the trench is carried out by thermal oxidation (5a) of the silicon. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thermal oxidation of Numazawa in order to use an efficient and inexpensive means at filling the trench that is proven to form a reliable film.

With regard to claim 15, Jang teaches in figure 1b wherein the step of amorphizing includes amorphizing the single-crystal lattice around a periphery of the recess so as to be self-aligned with the trench.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1 – 10, 15 and 17 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 13 – 19 of copending Application No. 10/466,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the features of the pending claims are covered in Application No. 10/466,145 claims. The pending claims cover the subject matter of the Application No. 10/466,145 claims, while the Application No. 10/466,145 claims are more specific.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. Claims 1 – 10, 15 and 17 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6 – 13 of copending Application No. 10/716,249. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the features of the pending claims are covered in the Application No. 10/716,249 claims. The pending claims cover the subject matter of the Application No. 10/716,249 claims, while the Application No. 10/716,249 claims are more specific.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Terminal Disclaimer

8. The terminal disclaimer filed on October 24, 2003 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of United States Patent number 6,537,873 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Response to Arguments

9. Applicant's arguments filed April 14, 2004 have been fully considered but they are not persuasive.

10. With regard to applicant's argument that "one skilled in the art, by combining the teachings of Kircher with Jang, results in depositing a layer of amorphous material on a crystallized structure, not an amorphous structure because the amorphous region is immediately crystallized. See Jang at col. 2, lines 52-54," it should be noted that Jang does not teach that the thermal treatment immediately occurs after the amorphization. Kircher teaches a thermal treatment following the deposition of an amorphous layer. Thus, one of ordinary skill in the art when viewing the teaching of Kircher and Jang would perform steps including the amorphization of Jang and the deposition of an amorphous layer of Kircher before any thermal process. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

1. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "where the amorphous material is deposited directly on the substrate") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II